UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,488	03/12/2004	Hsi-Chih Peng	14233.68	8392

21999 7590 11/27/2007

KIRTON AND MCCONKIE
60 EAST SOUTH TEMPLE,
SUITE 1800
SALT LAKE CITY, UT 84111

EXAMINER	
HOANG, THAI D	
ART UNIT	PAPER NUMBER
2616	
MAIL DATE	DELIVERY MODE
11/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,488	PENG ET AL.	
	Examiner	Art Unit	
	Thai D. Hoang	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-8,10,11 and 13-15* is/are rejected.

7)☒ Claim(s) *2-4,9 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5-8, 10-11, 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu et al, US Patent No. 6,442,137, hereinafter referred to as Yu.

Regarding claim 1, Yu discloses a system and method of controlling network traffic data in a full-duplex switched network operating according to Ethernet protocol. The switched network comprises a clock signal generator for generating the clock signal (clock multiplexer 104 generates a signal for scaling a transmit clock 100 and a receive clock 102, see fig. 4, col. 10, lines 1-5) , and a plurality of input/output ports for communicating therevia with at least one network node (see fig. 1, ports 24, 30, and 20s for communicating with network nodes 22, 12, and 14). The system further comprising the steps of:

asserting a control signal to the clock signal generator according to a certain condition of the input/output ports (a scheduler 80 signals to the clock multiplexer 104 according to assigned memory access slots for a gigabit port 24 and an expansion port 30, col. 10, lines 30-41, col. 11, lines 49-51 and 57-61. The assigned memory access

slots is based on detected network traffic conditions on the network switch ports, see col. 1, lines 64-66, abstract); and

adjusting the frequency of the clock signal outputted from the clock signal generator in response to the control signal (the clock multiplexer 104 adjusts its output clock signal based on the received signal from the scheduler 80, see col. 10, lines 30-41 and 45-48, col. 11, lines 49-51 and 57-61).

Regarding claim 5, Yu discloses the certain condition of the input/output ports is data transmission rates of the input/output ports in use (the clock multiplexer 104 configured to selectively change a data rate based on the number of assigned memory slots assigned to a first and a second ports, abstract, and col. 2, lines 35-39, col. 11, lines 46-61.)

Regarding claims 6, 10 and 13, Yu discloses the certain condition of the input/output ports is an overall data transmission rate of all the input/output ports connecting to network nodes (the scheduler 80 assigns each of the 10/100 Mb/s modules in the MAC 20 a fixed grant of bandwidth slots, and the scheduler 80 assigns the Gigabit port 24 and Expansion port 30 a respective initial number of slots from a bandwidth pool of slots, col. 9, lines 28-43.)

Regarding claim 7, Yu discloses the method comprising the steps of:

generating a first clock signal with a first frequency in response to a first control signal corresponding to a first overall data transmission rate of the input/output ports (the scheduler 80 initially assigns a first number of memory access slots to the Gigabit port 24, and a second number of memory access slots to the Expansion port 30 (see

fig. 5, step S1, col. 9, lines 36-43, col. 10 lines 52-55). Since the clock multiplexer 104 controls data rate of the gigabit port 24 and expansion port 30 (col. 10, lines 1-41, col. 11, lines 49-51 and 57-61); therefore, the clock multiplexer 104 inherently generates a first clock signal corresponding to the assigned memory access the gigabit port 24 and expansion port 30, herein the assigned memory access slots, as explained above in claim 1, is based on detected network traffic conditions on the network switch ports, see col. 1, lines 64-66, abstract);

generating a second clock signal with a second frequency higher than the first frequency in response to a second control signal corresponding to a second overall data transmission rate of the input/output port higher than the first overall data transmission rate (when the scheduler Expansion port 30 receives a larger number of memory access slots, the data rate of the port can be increased to accommodate the larger data rate capacity. Hence, the clock multiplexer 104 has to generate a higher frequency clock to increase the data rate of the Expansion port 30 based on the control signal received from the scheduler 80, see fig. 5, step S3, col. 10, lines 34-41, and col. 11, lines 49-51); and

generating a third clock signal with a third frequency lower than the first frequency in response to a third control signal corresponding to a third overall data transmission rate of the input/output port lower than the first overall data transmission rate (If the scheduler 80 determines the Gigabit port 24 is encountering more network traffic than the Expansion port 30, the scheduler 80 signals to the clock multiplexer 104

generating a third clock frequency, that sets the data rate of the Expansion port 30 at a lower data rate, see Fig. 5, step S5, col. 11, lines 57-61.)

Regarding claim 8, Yu discloses a system and method of controlling network traffic data in a full-duplex switched network operating according to Ethernet protocol. The switched network comprises a clock signal generator for generating the clock signal (clock multiplexer 104 generates a signal for scaling a transmit clock 100 and a receive clock 102, see fig. 4, col. 10, lines 1-5), and a plurality of input/output ports for communicating with a plurality of network nodes (see fig. 1, ports 24, 30, and 20s for communicating with network nodes 22, 12, and 14). The system further comprising the steps of:

detecting connection states of the input/output ports with the plurality of network nodes (the scheduler 80 assigns each of the 10/100 Mb/s modules in the MAC 20 a fixed grant of bandwidth slots, and the scheduler 80 assigns the Gigabit port 24 and Expansion port 30 a respective initial number of slots from the bandwidth pool, col. 9, lines 28-43);

adjusting the frequency of the clock signal according to the connection states of the input/output ports with the plurality of network nodes (the clock multiplexer 104 adjusts its output clock signal based on assigned slots for the Gigabit port 24 and Expansion port 30 to communicate with network nodes 12, 22, see col. 10, lines 30-41 and 45-48, col. 11, lines 49-51 and 57-61);

repeating the detecting and adjusting steps at intervals of a predetermined period (see fig. 5, if "End of sequence cycle" at step S4 or S6 is "Yes", repeat step S2 to detect traffic status at ports 24 and 30, and then adjust clock at step S3 or S5.)

Regarding claim 11, Yu discloses the system comprising:

a first number of input/output ports for connecting to a variable number of network nodes (see fig. 1, network nodes 12, 22, 14 connect to a switch 12a over ports 30, 24 and 20s) the variable number being equal to or less than the first number (the number of network nodes 12, 22, 14 connected to the switch 12a has to equal or less than number of ports 30, 24 and 20s);

a connection-state detector in communication with the first number of input/output ports, detecting connection states of the input/output ports with the variable number of network nodes (the scheduler 80 assigns each of the 10/100 Mb/s modules in the MAC 20 a fixed grant of bandwidth slots, and the scheduler 80 assigns the Gigabit port 24 and Expansion port 30 a respective initial number of slots from the bandwidth pool, col. 9, lines 28-43), and asserting a control signal according to the connection states of the input/output ports (a scheduler 80 signals to the clock multiplexer 104 according to assigned slots for the gigabit port 24 and expansion port 30, col. 10, lines 30-41, col. 11, lines 49-51 and 57-61); and

a clock signal generator generating a clock signal having a frequency determined according to the control signal (the clock multiplexer 104 generates a clock frequency based on the signal received from the scheduler 80; col. 10, lines 30-41 and col. 11, lines 49-51 and 57-61.)

Regarding claim 15, Yu disclose the clock signal generator and the connection state detector are integrated in a control chip (the switch 12 is integrated in a single chip, col. 3, lines 41-43, and col. 4, line 67- col. 5, line 1; therefore, the scheduler 80 and the clock multiplexer 104 are integrated in a single chip.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu as shown above in view of Tang US Patent No. 6, 298,067 B1, hereinafter referred to as Yu and Tang respectively.

Regarding claim 14, Yu does not disclose the clock signal generator is a phase-locked loop (PLL) clock signal generator. However, Tang discloses a Distributed arbitration scheme for network device, wherein a buffered distributor within a hub comprises clock generators 400 using the Phase locked loop (PLL) technique, see fig. 4, col. 5, lines 44-47. It would have been obvious to one of ordinary skill in the art at the time the invention was made to adapt the PLL disclosed by Tang into Yu's system in order to stabilize frequencies in an integrated circuit.

Allowable Subject Matter

Claims 2-4, 9, and 12, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kang et al., US PG-PUB No. 2004/0090995 A1, "Ethernet switching apparatus and method using frame multiplexing and demultiplexing."

Levy et al., Patent No. US 6,317,804 B1, "Concurrent serial interconnect for integrating functional blocks in an integrated circuit device."

Tang et al., US Patent No. 6,256,320 B1, "Dual clocks for network device."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai D. Hoang whose telephone number is (571) 272-3184. The examiner can normally be reached on Monday-Friday 10:00am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thai Hoang
Art Unit 2616